Regulators, Dampers and Clock Non Idealities in Time Sensitive Networks

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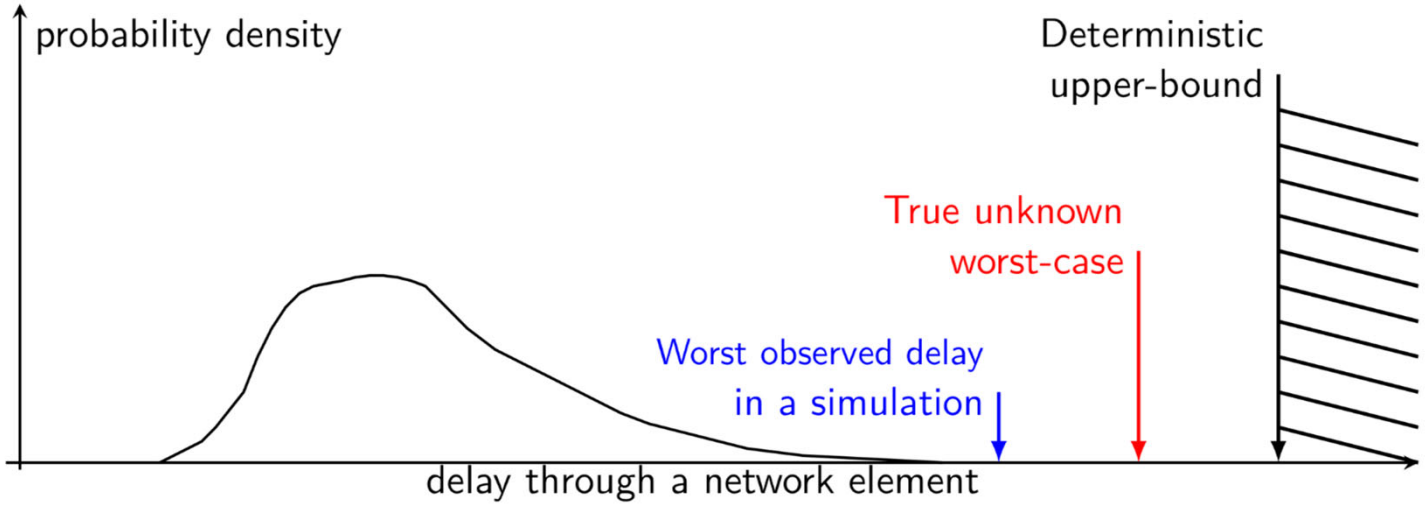
Per-Class Time Sensitive Networks

1. Flows are assigned to a small number of classes with different quality of service requirements
2. Every flow is constrained at the source by an *arrival curve* (e.g. with rate r and burstiness b, #bits sent over any interval of any duration t is $\leq rt+b$)
3. At every node, traffic of a given class is FIFO and is assured to receive a minimum amount of service (e.g. with rate R and latency T)

⇒ Deterministic delay, delay jitter and backlog bounds can be derived using network calculus



Burstiness Cascade

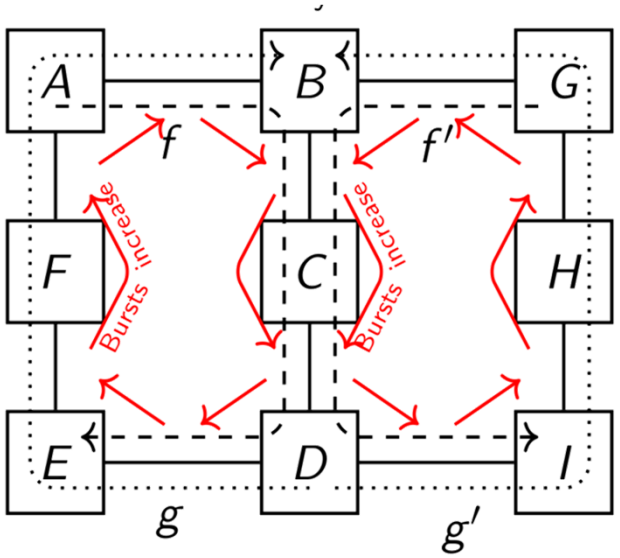
Unlike in a per-flow network, in a per-class network with FIFO inside every class, burstiness of every flow increases at every hop as a function of other flows' burstiness: e.g.

$$b_f^* = b_f + r\left(T + \frac{b_{tot} - b_f}{R}\right)$$

Increased burstiness causes increased burstiness (cascade).

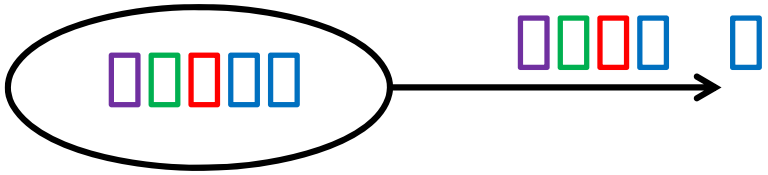
Computing burstiness requires solving a fixpoint.

Good delay bounds depend on the topology and on the number of hops. In non-feedforward topologies, delay bounds can be bad even at medium utilizations. [Bennett 2002].



Instability (infinite bounds) can occur even at low utilization [Andrews 2009].

Regulators in Time Sensitive Networks



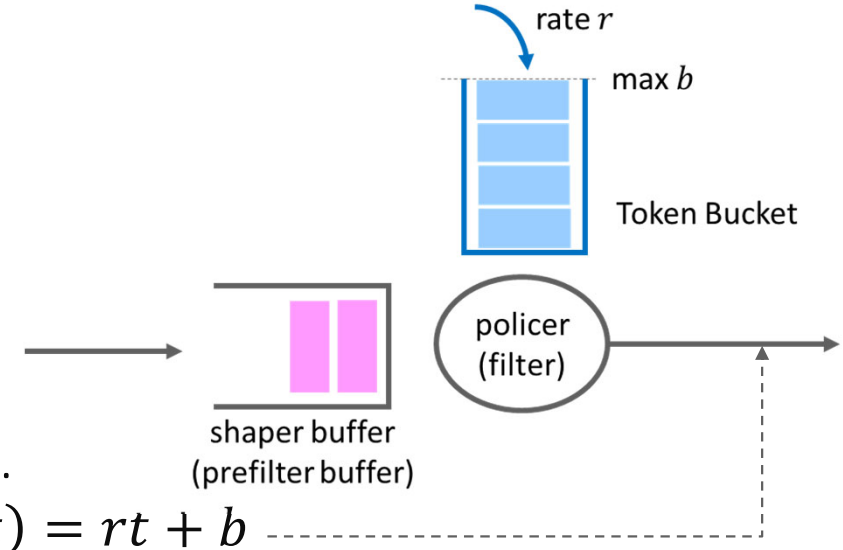
Regulator (= shaper) delays packets in order to limit burstiness to a prescribed value (i.e. enforces an arrival curve constraint).

Example: Token Bucket filter (Linux tc; IEEE TSN ATS).

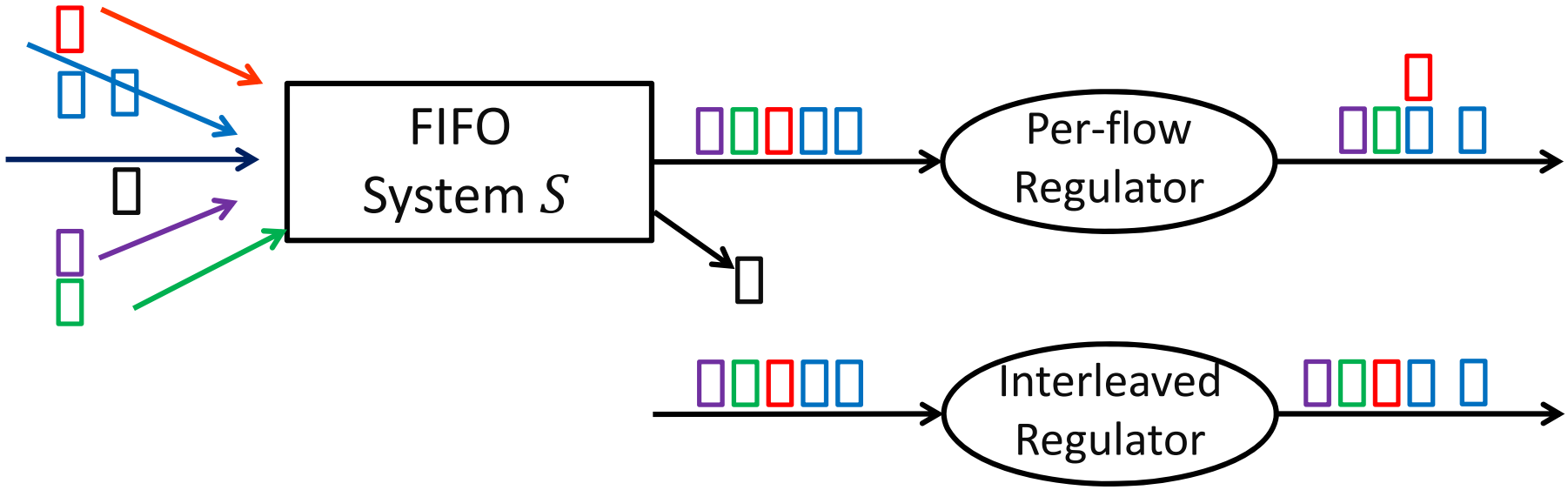
Imagine a token bucket, spontaneously replenished at rate r up to some maximum b.

In order to be released, a packet must consume same amount of tokens as its size.

If there are not enough tokens, packet must wait.
As soon as there are enough tokens, packet is released.
This is the regulator for the arrival curve constraint $\alpha(t) = rt + b$



Regulators Avoid Cascading Burstiness in Per-Class Networks

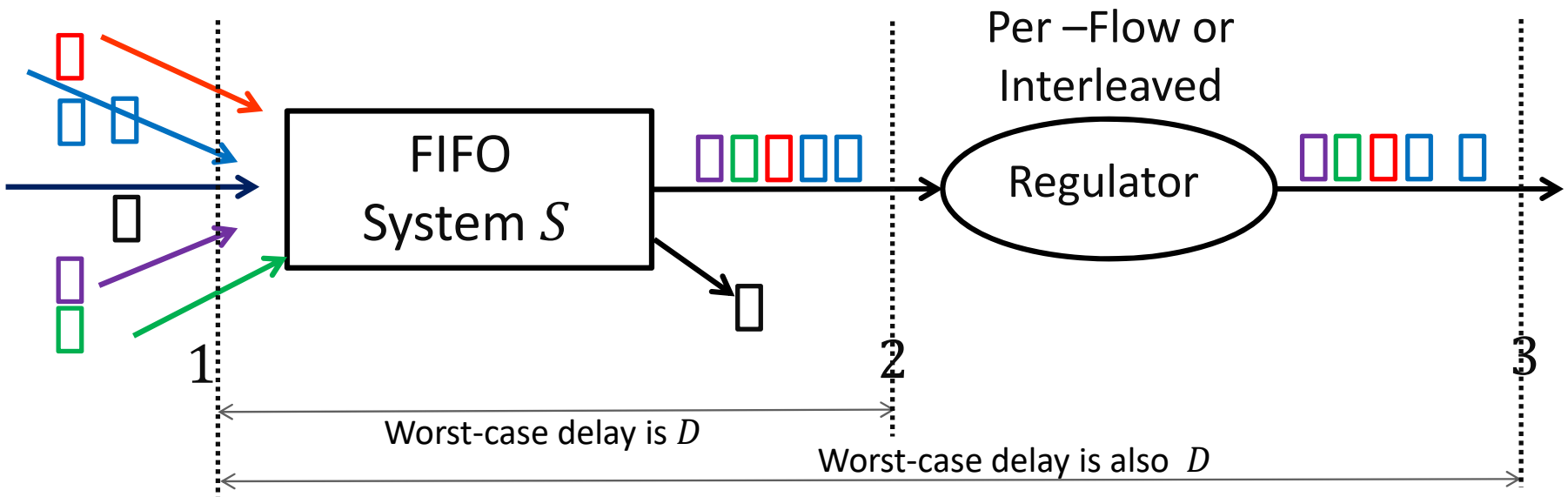


Per flow regulator: one state + one queue per flow.

Interleaved regulator: one state per flow + one global queue:

- packet at head of queue is examined against the arrival constraint (e.g. rate r_f and burstiness b_f) of its flow f; this packet is delayed if it came too early; different flows in same queue can have different arrival constraints;
- packets not at head of queue wait for their turn to come [Specht-Samii 2016].

Regulators do not Increase Worst Case Delay



Assume S is FIFO per flow (per-flow regulator) or globally (interleaved regulator).

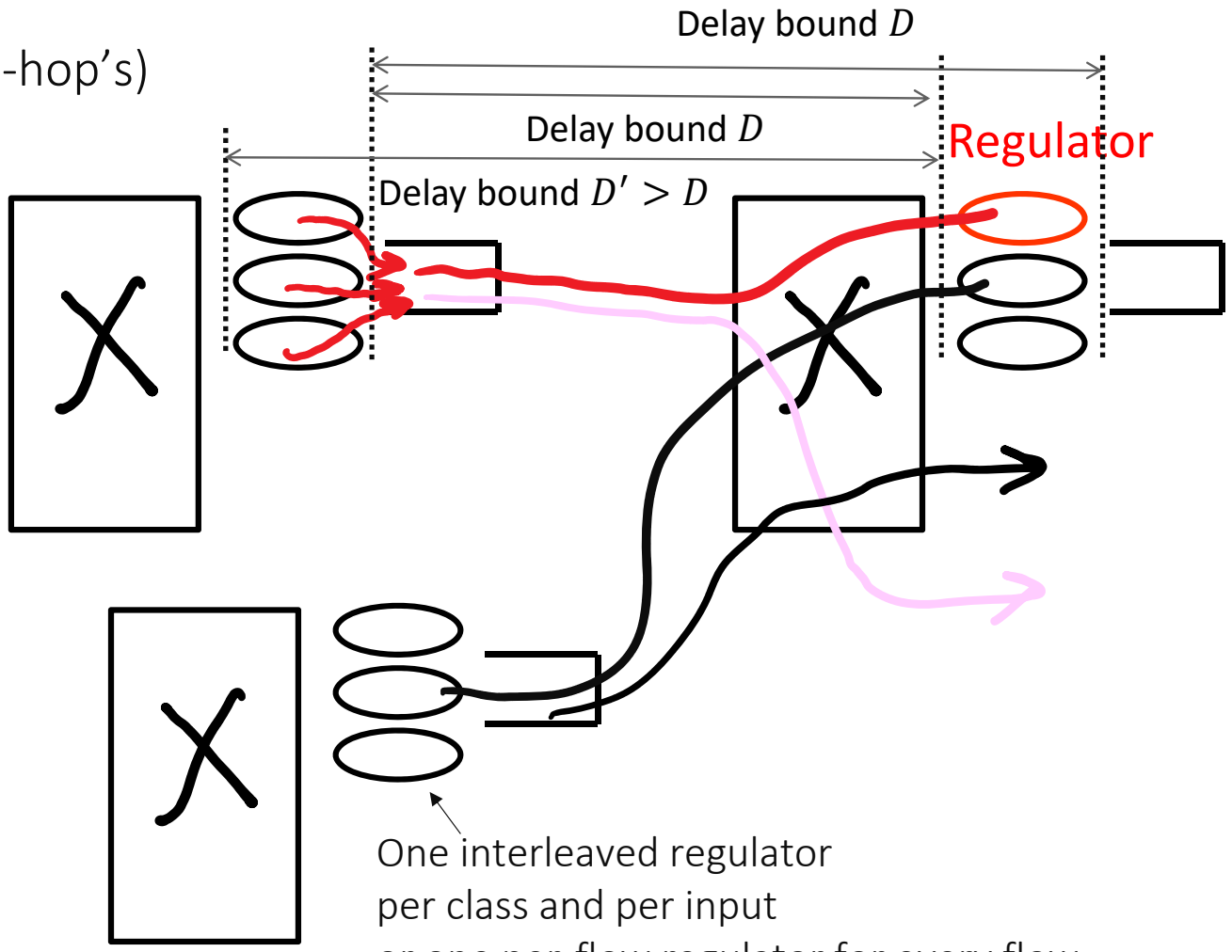
Assume every flow satisfies some arrival constraint at 1 (e.g. rate and burstiness) and regulators enforces same constraint at 3.

The worst case delay $1-3$ is the same as the worst-case delay $1-2$ [Le Boudec 2018].

Network With Regulators [IEEE TSN ATS]

- Regulators are integrated in (next-hop's) queuing system.
- Worst case end-to-end queuing delay can ignore regulators. Worst-case delay at one regulator is absorbed by delay bound at previous hop.
- Queuing delay and backlog at every hop can be computed easily since traffic is regulated.

[Mohammadpour 2018]



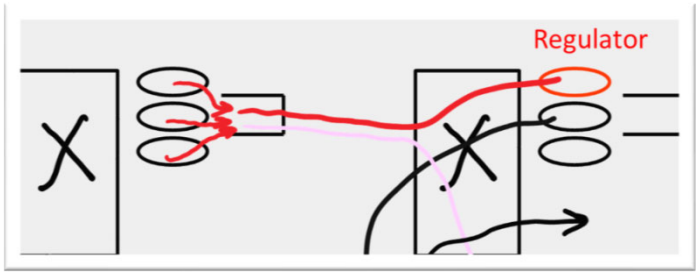
Clock Non Idealities

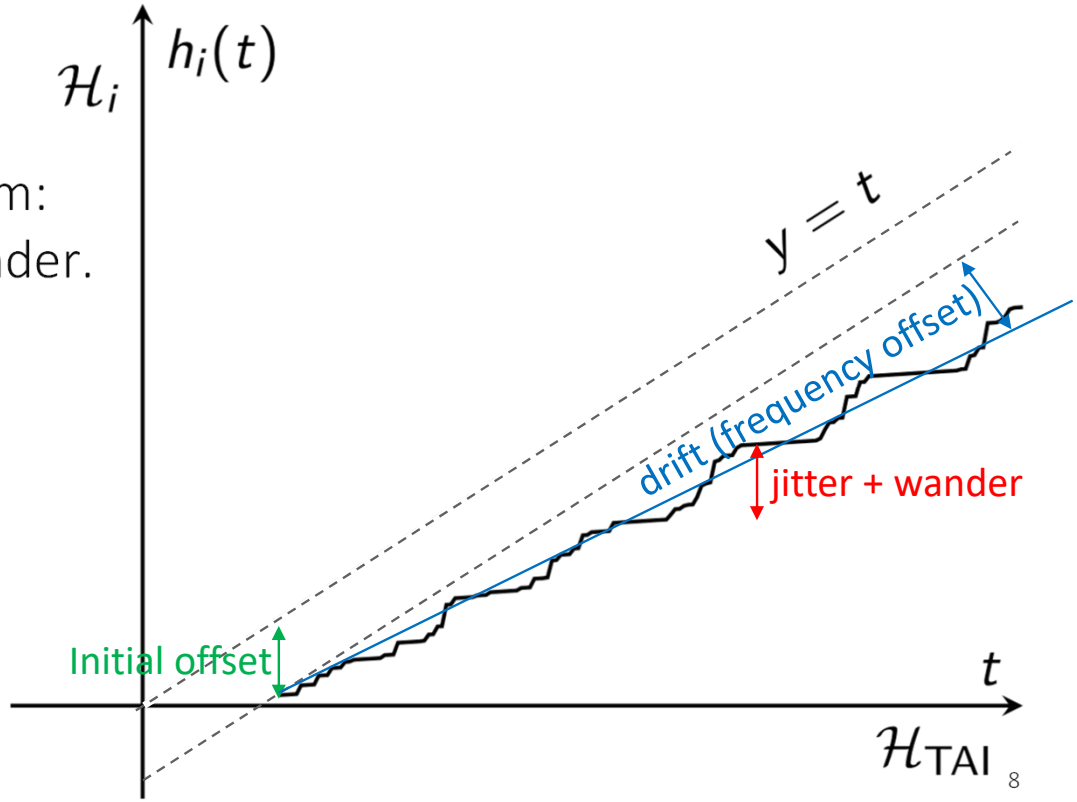
Previous theory assumes perfect time everywhere.

In reality, nodes use local clocks that are not ideal.

- tight sync (PTP, White Rabbit, GPS) : timestamping error $\leq \omega \approx$ 10ns–1μs
- loose sync (NTP): $\omega \approx$ 1ms – 1s
- no sync: timestamping error ω unbounded; measurement of time interval on same system: error is bounded by clock drift, jitter and wander.

[ITU 1996]





Regulators use time measurements to decide when a packet can be released.

What is the effect of clock non ideality ?

Clock Model in Network Calculus [Thomas 2020]

A delay measurement is performed with one clock → d and with another clock → d'

Time synchronization error: $d' - d \leq 2\omega$

Clock jitter and wander: $d' \leq \rho d + \eta$

This gives the constraints

$$-\min\left(\left(1-\frac{1}{\rho}\right)d + \frac{\eta}{\rho}, 2\omega\right) \leq d' - d \leq \min((\rho-1)d + \eta, 2\omega)$$

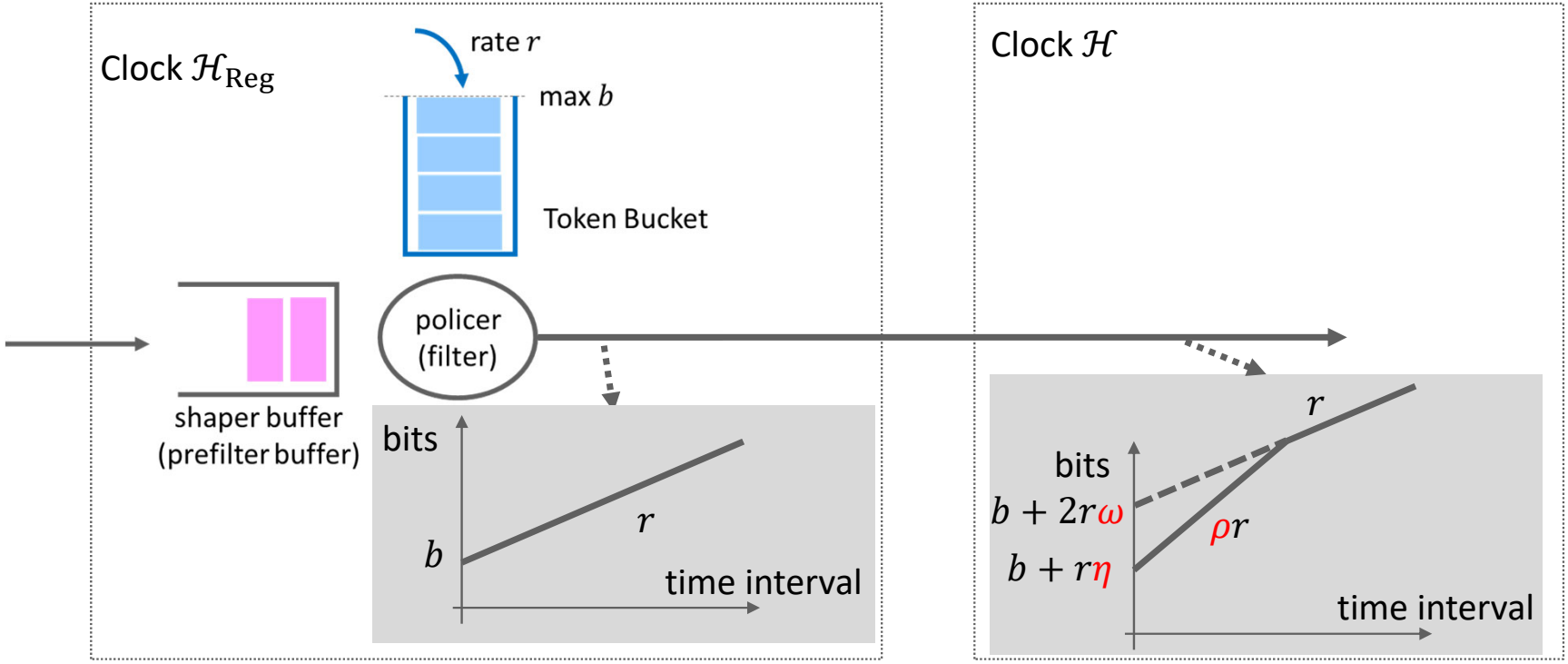
- $\omega =$ time error bound = 1μs in TSN with PTP; = $+\infty$ if no synchronization
- $\rho =$ clock-stability bound =1.0001; $\eta =$ timing-jitter bound = 2ns (e.g. in TSN)

Model is symmetric, i.e. same inequalities if we exchange $d' \leftrightarrow d$

Change of Clock: Arrival Curves

Assume a flow satisfies a token bucket constraint (r, b) when observed with clock $\mathcal{H}_{\text{Reg}}$
i.e. arrival curve constraint $\alpha^{\mathcal{H}_{\text{Reg}}}(t) = rt + b$

When observed with some other clock $\mathcal{H}$, it satisfies the arrival curve constraint
$\alpha^{\mathcal{H}}(t) = \min(\rho rt + b + r\eta\,, rt + b + 2r\omega)$ [Thomas 2020]



Consequences for Non-Adapted Regulators

Non adapted regulator : uses same nominal arrival curve as at source.

Perfect clocks:

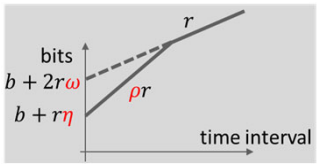
- Regulator does not increase worst-case delay

Non-synchronized network:

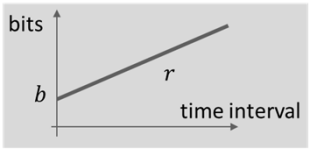
- Per-flow and interleaved regulator unstable (unbounded delay).

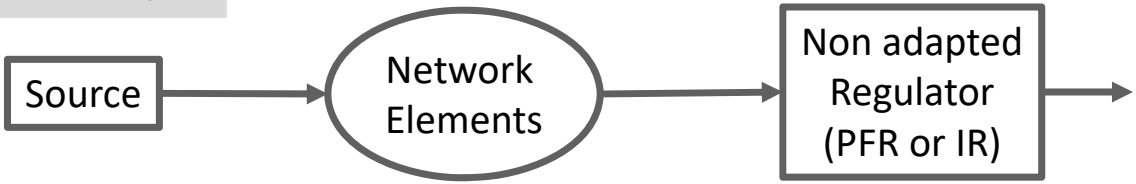
Synchronized network:

- Per-flow regulator incurs delay penalty up to 4ω;
- Interleaved regulator is unstable.



In regulator's clock, flow satisfies this constraint at source



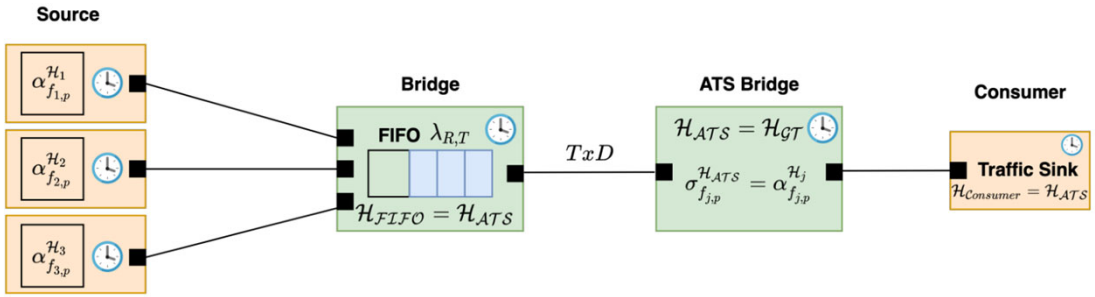


Flow constrained by $\alpha(t) = rt + b$ in local clock

Implements constraint $\alpha(t) = rt + b$ in local clock

Synchronized clocks,
Unstable non-adapted Interleaved Regulator (= IEEE TSN ATS)

ns-3 simulations with adversarial clocks



3 sources @ 147 kb/s

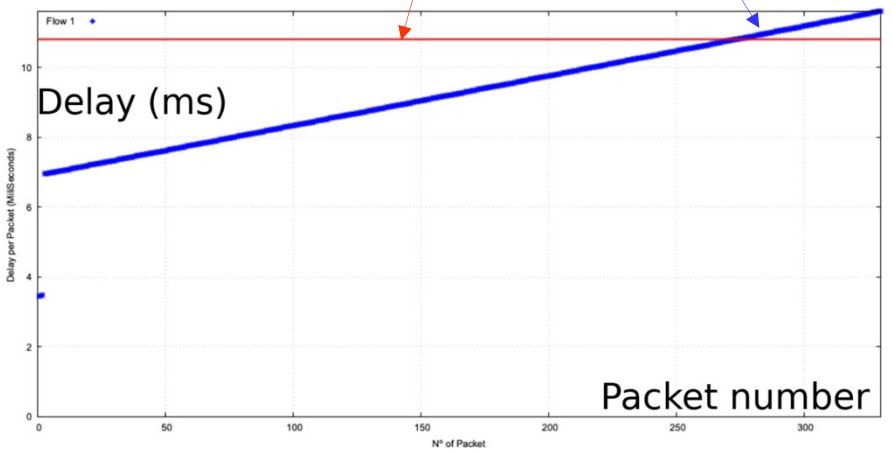
$\omega = 1\mu s, \rho = 1.0001$

Delay increases by up to 100μs per second of operation.

[Thomas 2020]

Delay bound ignoring clock non ideality

Actual packet delay

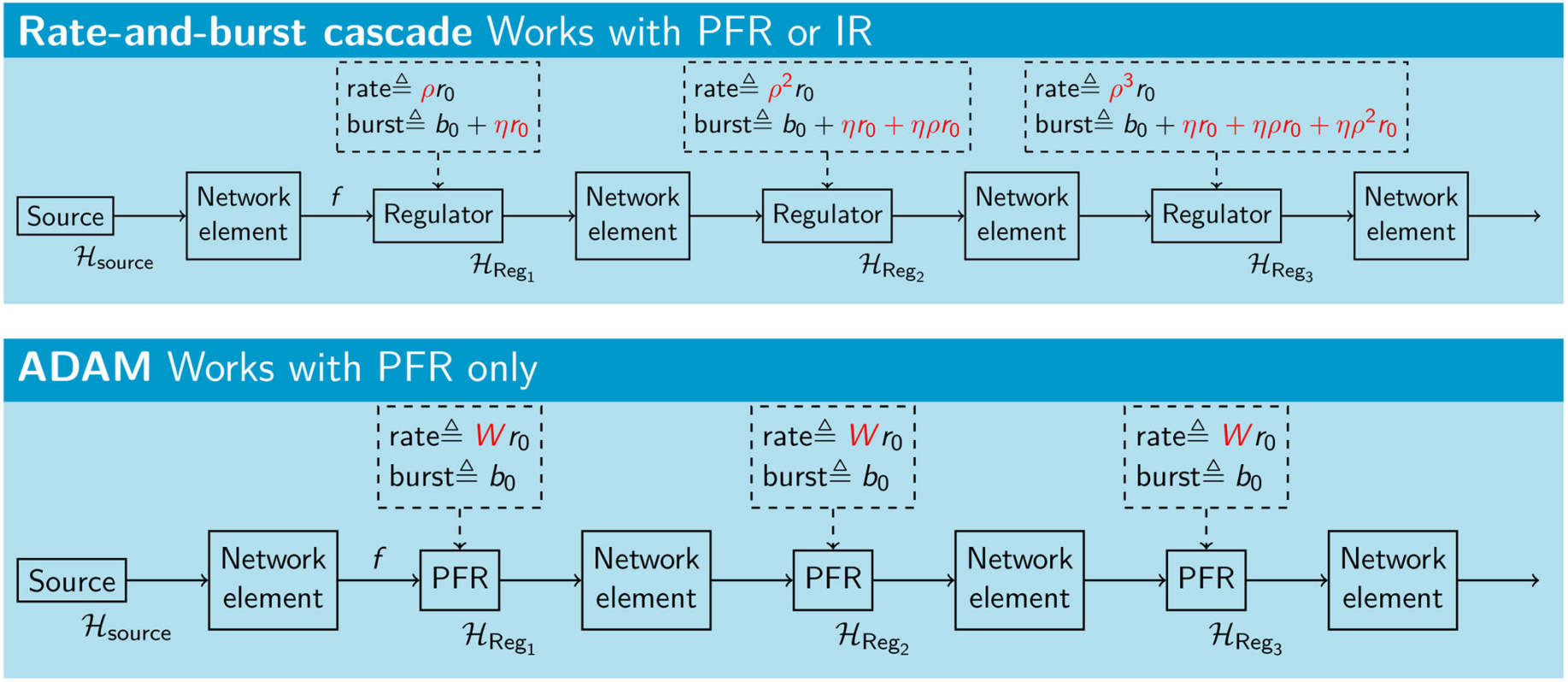


Work by Guillermo Aguirre

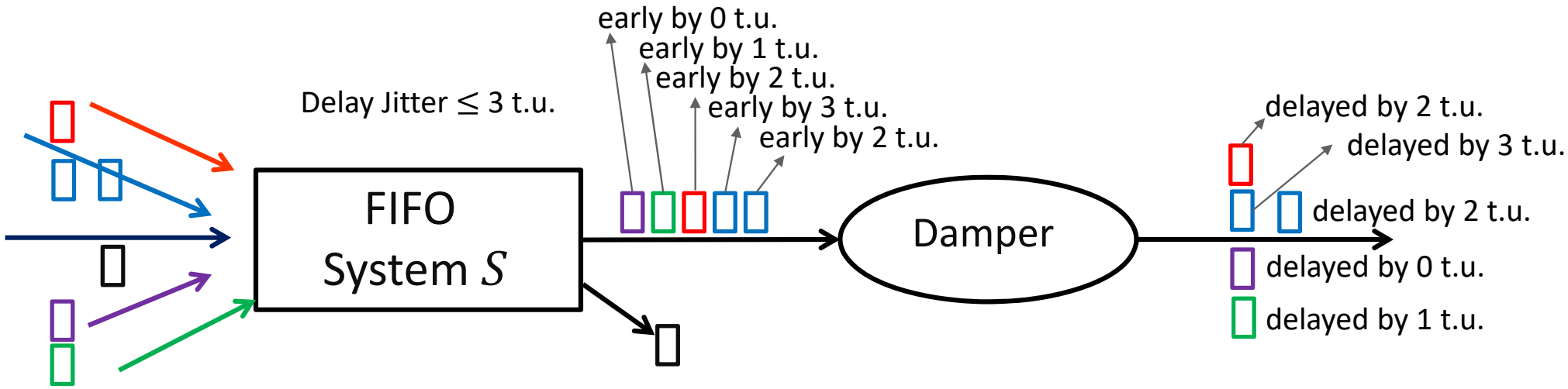
Regulators are sensitive to clock inaccuracies

In tighty synchronized networks, IR must be adapted otherwise is unstable; PFR need not be adapted but increased delay due to clock inaccuracy must be accounted for. In loosely synchronized or non synchronized networks, both PFR and IR must be adapted.

Examples of adaptation methods



Beyond Regulators: Dampers



Damper delays a packet by "earliness" read from packet header.

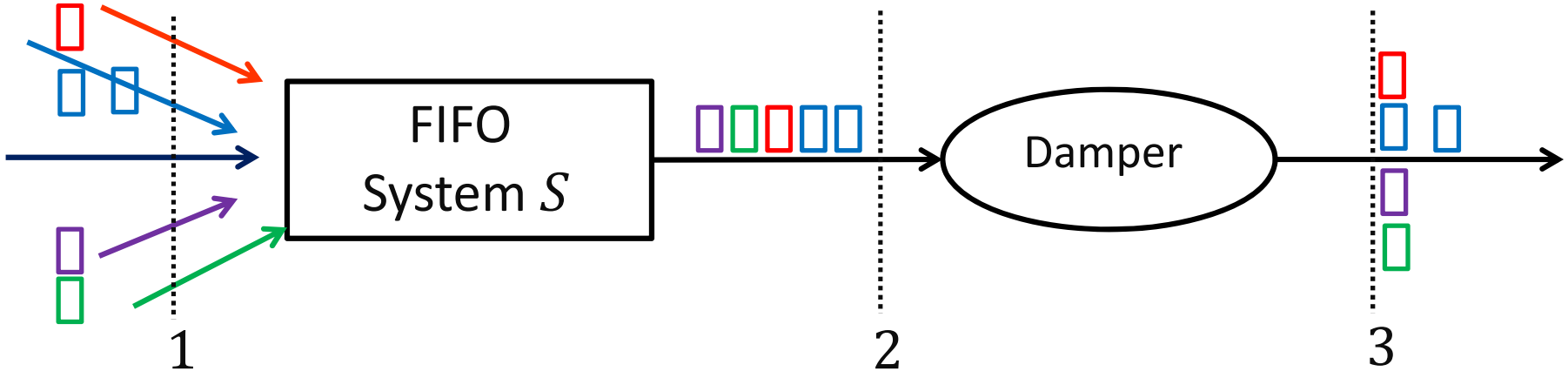
Removes (almost all) jitter.

Like a regulator, does not exist in isolation, is combined with queue at next hop.

Unlike regulator, is stateless.

[Cruz 1998] RCSP [Zhang 1993], RGCQ [Shoushou 2020], ATS with Jitter Control [Grigorjew 2020].

Dampers solves Burstiness Cascade Problem



Delay jitter $1 \rightarrow 3$ is 0 in theory; in practice, a small residual delay jitter $\leq \Delta$ (in true time):

At 1: assume a flow is constrained by token bucket with rate r and burstiness b (in true time);

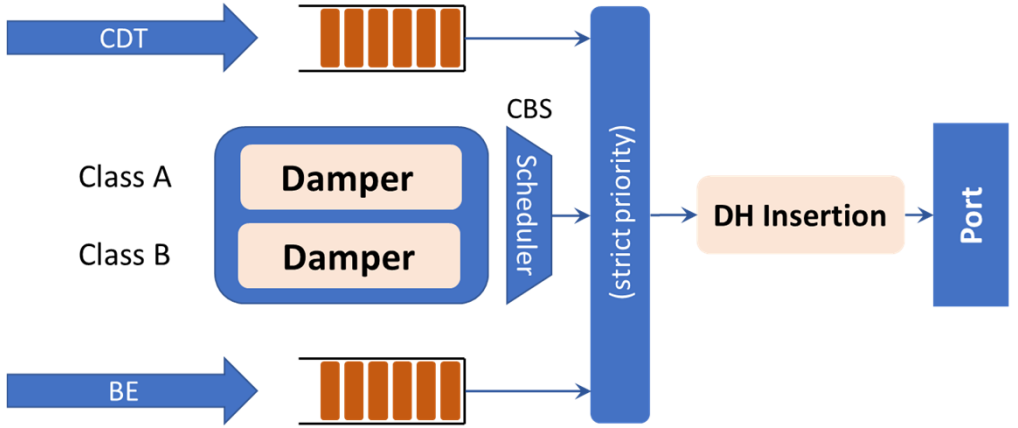
$\Rightarrow$ At 3, same flow is constrained by token bucket with rate r and burstiness $b + r\Delta$ (in true time).

Tolerance Δ depends on jitter implementation and not on traffic
$\Rightarrow$ no burstiness cascade.

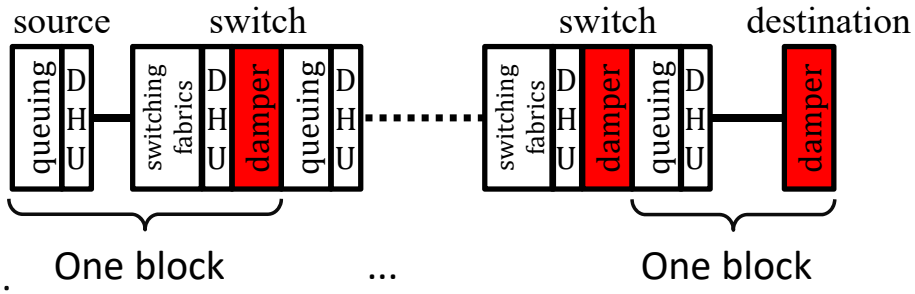
Damper in an IEEE TSN Switch

Damper replaces the FIFO queue
of the credit-based shaper.

Makes packet visible to the scheduler at its theoretical eligibility time ± some *damper tolerance.*



Damper Header inserted on the transmission line.



Example: RCSP damper;
with clock model in [Thomas 2020] : residual jitter
1.264 μs per block, with or without clock synchronization
timing accuracy and clock non idealities contributes to 262 ns [Mohammadpour 2021].

Conclusion

Time Sensitive Networks require deterministic, proven delay, jitter and backlog bounds.

Network Calculus provides theory and tools for computing such bounds and for understanding operation of regulators. We extended it to account for clock non-idealities.

Regulators must be adapted to account for clock non-idealities.

Beyond regulators, dampers are stateless and are less affected by clock non-idealities.

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